AMENDMENTS TO THE SPECIFICATION:

Please replace the Title with the following replacement Title:

-- AN INSTRUCTION-PIPELINE INSTRUCTION QUEUE FOR INSTRUCTION REISSUE --.

Please replace the abstract of the disclosure with the following amended abstract:

[[An]] With respect to a microprocessor including an instruction pipeline ~~in a microprocessor, comprising~~ that includes a plurality of pipeline units ~~with each of the pipeline units~~ to which instructions are distributed for processing ~~instructions~~ in multiple threads, the instruction pipeline, and a method of processing instructions therein, from an upstream pipeline unit, instructions on a thread are issued. At least one of the plurality of pipeline units receives the instructions from another of the pipeline units, stores the instructions, passes the instructions to a downstream pipeline unit, detects a stall that occurs in the instruction pipeline, and, after the stall is detected, reissues to the downstream pipeline unit at least one of the instructions that had been previously issued to the downstream pipeline unit ~~after a stall occurs in the instruction pipeline~~.